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FINAL

Jameco Part Number 111780

# Am27C040

## 4 Megabit (512 K x 8-Bit) CMOS EPROM

## DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — Available in speed options as fast as 90 ns
- **Low power consumption**
  - — <10 µA typical CMOS standby current
- **JEDEC-approved pinout**
  - — Plug-in upgrade for 1 Mbit and 2 Mbit EPROMs
  - — Easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance standard**
- **100% Flashrite™ programming**
  - — Typical programming time of 1 minute
- **Latch-up protected to 100 mA from –1 V to $V_{CC}$ + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, PLCC packages**

## GENERAL DESCRIPTION

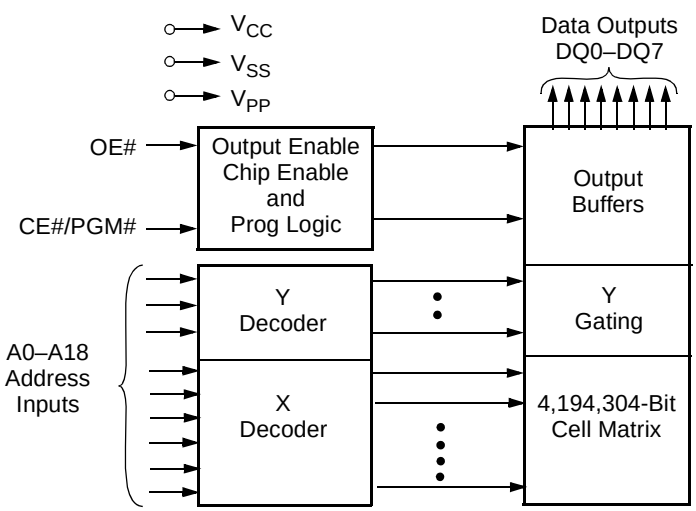
The Am27C040 is a 4 Mbit ultraviolet erasable programmable read-only memory. It is organized as 512K bytes, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The device is available in windowed ceramic DIP packages and plastic one-time programmable (OTP) packages.

Data can be typically accessed in less than 90 ns, allowing high-performance microprocessors to operate without any WAIT states. The device offers separate Output Enable (OE#) and Chip Enable (CE#) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 50 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The device supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming time of 1 minute.

## BLOCK DIAGRAM




14971H-1

Publication# **14971** Rev: **H** Amendment/**0**
Issue Date: **August 25, 1999**

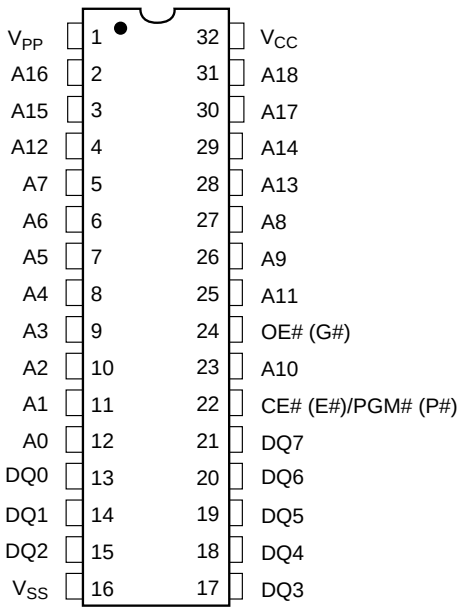
## PRODUCT SELECTOR GUIDE

| Family Part Number | Am27C040 | | | |
|---|---|---|---|---|
| Speed Options ($V_{CC}$ = 5.0 V ± 10%) | **-90** | **-120** | **-150** | **-200** |
| Max Access Time (ns) | 90 | 120 | 150 | 200 |
| CE# (E#) Access (ns) | 90 | 120 | 150 | 200 |
| OE# (G#) Access (ns) | 40 | 50 | 65 | 75 |

## CONNECTION DIAGRAMS

### Top View

**DIP**

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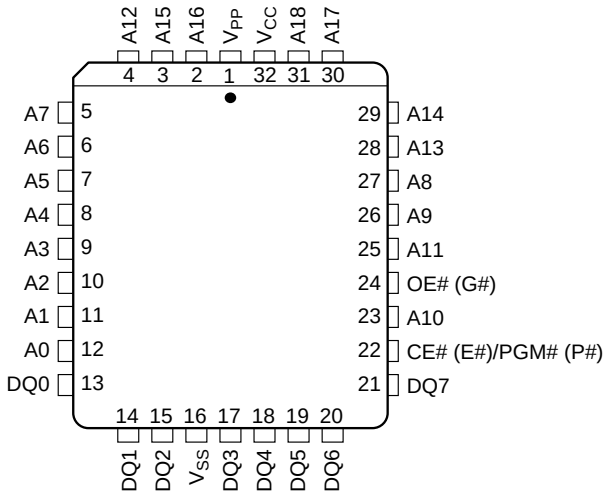
**PLCC**




14971H-3

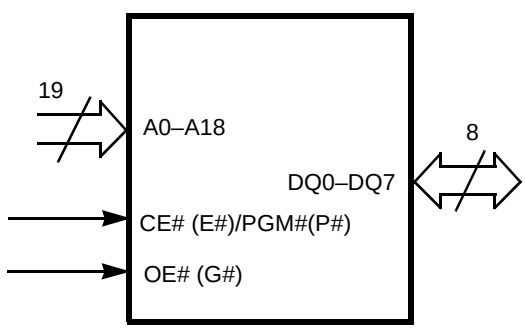
***Notes:***

1. *JEDEC nomenclature is in parenthesis.*
2. *The 32-pin DIP to 32-pin PLCC configuration varies from the JEDEC 28-pin DIP to 32-pin PLCC configuration.*

## PIN DESIGNATIONS

| | | |
|---|---|---|
| A0–A18 | = | Address Inputs |
| CE# (E#)/PGM# (P#) | = | Chip Enable/Program Enable Input |
| DQ0–DQ7 | = | Data Inputs/Outputs |
| OE# (G#) | = | Output Enable Input |
| $V_{CC}$ | = | $V_{CC}$ Supply Voltage |
| $V_{PP}$ | = | Program Voltage Input |
| $V_{SS}$ | = | Ground |

## LOGIC SYMBOL

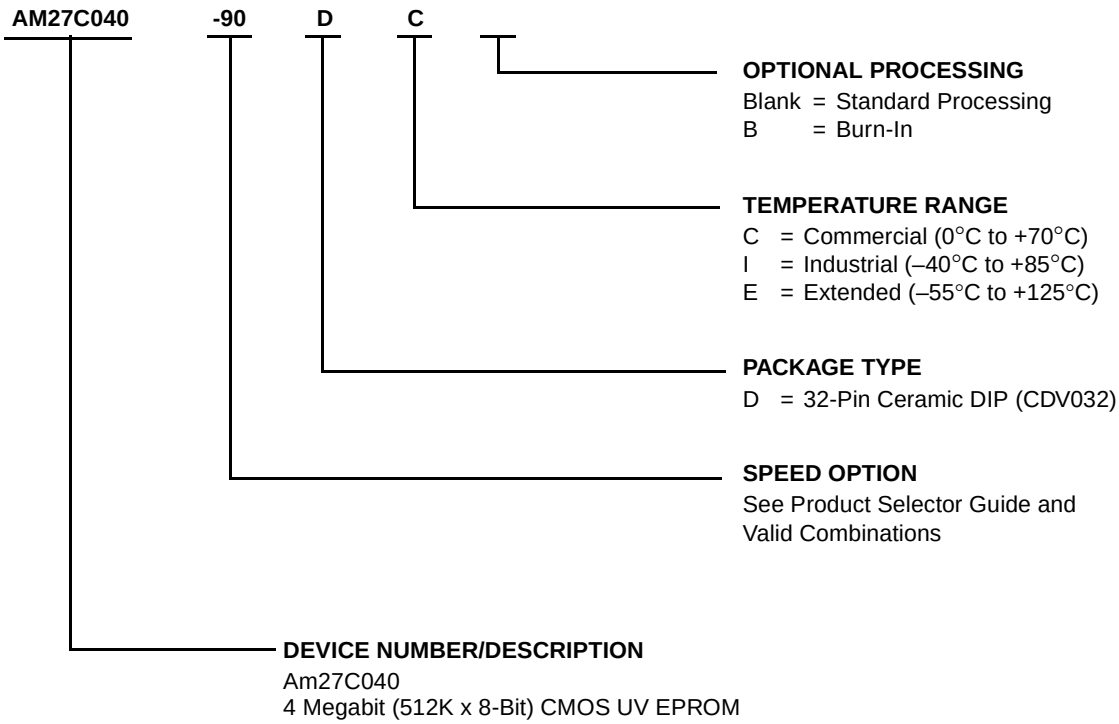



14971E-4

## ORDERING INFORMATION

### UV EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | |
|---|---|
| AM27C040-90 | DC, DCB, DI, DIB, DE, DEB |
| AM27C040-120 | |
| AM27C040-150 | |
| AM27C040-200 | |

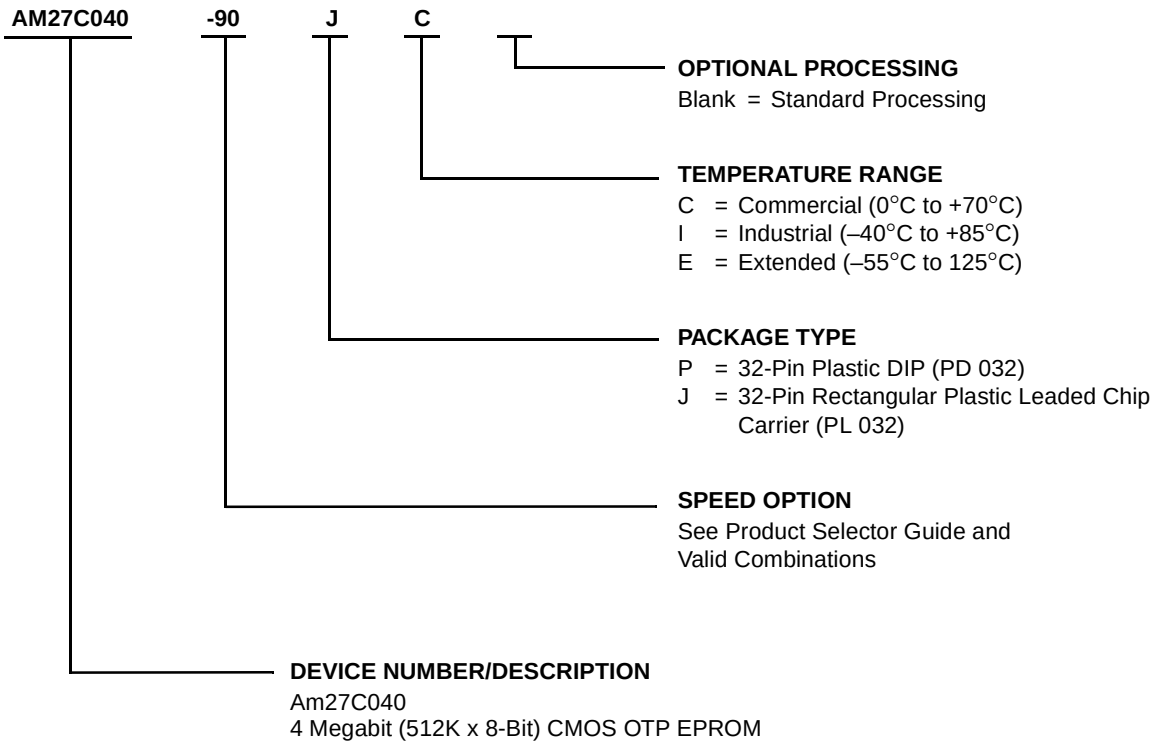
**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## ORDERING INFORMATION

### OTP EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | |
|---|---|
| AM27C040-90 | PC, PI, JC, JI |
| AM27C040-120 | |
| AM27C040-150 | |
| AM27C040-200 | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

### Device Erasure

In order to clear all locations of their programmed contents, the device must be exposed to an ultraviolet light source. A dosage of 30 W seconds/cm$^2$ is required to completely erase the device. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Å — with intensity of 12,000 µW/cm$^2$ for 30 to 35 minutes. The device should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

Note that all UV erasable devices will erase with light sources having wavelengths shorter than 4000 Å, such as fluorescent light and sunlight. Although the erasure process happens over a much longer time period, exposure to any light source should be prevented for maximum system reliability. Simply cover the package window with an opaque label or substance.

### Device Programming

Upon delivery, or after each erasure, the device has all of its bits in the “ONE”, or HIGH state. “ZEROs” are loaded into the device through the programming procedure.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the $V_{PP}$ pin, CE#/PGM# is at $V_{IL}$ and OE# is at $V_{IH}$.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart in the EPROM Products Data Book, Programming section (Section 5, Figure 5-1) shows AMD’s Flashrite algorithm. The Flashrite algorithm reduces programming time by using a 100 µs programming pulse and by giving each address only as many pulses to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum pulses allowed is reached. This process is repeated while sequencing through each address of the device. This part of the algorithm is done at $V_{CC}$ = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to the EPROM Products Data Book, Section 5 for the programming flow chart and characteristics.

### Program Inhibit

Programming different data to multiple devices in parallel is easily accomplished. Except for CE#/PGM#, all like inputs of the devices may be common. A TTL low-level program pulse applied to one device’s CE#/PGM# input with $V_{PP}$ = 12.75 V ± 0.25 V will program that particular device. A high-level CE#/PGM# input inhibits the other devices from being programmed.

### Program Verify

A verification should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with OE# at $V_{IL}$, CE#/PGM# at $V_{IH}$, and $V_{PP}$ between 12.5 V and 13.0 V.

### Auto Select Mode

The autoselect mode provides manufacturer and device identification through identifier codes on DQ0–DQ7. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force $V_H$ on address line A9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from $V_{IL}$ to $V_{IH}$ (that is, changing the address from 00h to 01h). All other address lines must be held at $V_{IL}$ during the autoselect mode.

Byte 0 (A0 = $V_{IL}$) represents the manufacturer code, and Byte 1 (A0 = $V_{IH}$), the device identifier code. Both codes have odd parity, with DQ7 as the parity bit.

### Read Mode

To obtain data at the device outputs, Chip Enable (CE#/PGM#) and Output Enable (OE#) must be driven low. CE#/PGM# controls the power to the device and is typically used to select the device. OE# enables the device to output data, independent of device selection. Addresses must be stable for at least $t_{ACC}$–$t_{OE}$. Refer to the Switching Waveforms section for the timing diagram.

### Standby Mode

The device enters the CMOS standby mode when CE#/PGM# is at $V_{CC}$ ± 0.3 V. Maximum $V_{CC}$ current is reduced to 100 µA. The device enters the TTL-standby mode when CE#/PGM# is at $V_{IH}$. Maximum $V_{CC}$ current is reduced to 1.0 mA. When in either standby mode, the device places its outputs in a high-impedance state, independent of the OE# input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation, and
- Assurance that output bus contention will not occur

CE#/PGM# should be decoded and used as the primary device-selecting function, while OE# be made a

common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and $V_{SS}$ to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between $V_{CC}$ and $V_{SS}$ for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## MODE SELECT TABLE

| Mode | | CE#/PGM# | OE# | A0 | A9 | $V_{PP}$ | Outputs |
|---|---|---|---|---|---|---|---|
| Read | | $V_{IL}$ | $V_{IL}$ | X | X | X | $D_{OUT}$ |
| Output Disable | | $V_{IL}$ | $V_{IH}$ | X | X | X | HIGH Z |
| Standby (TTL) | | $V_{IH}$ | X | X | X | X | HIGH Z |
| Standby (CMOS) | | $V_{CC}$ + 0.3 V | X | X | X | X | HIGH Z |
| Program | | $V_{IL}$ | $V_{IH}$ | X | X | $V_{PP}$ | $D_{IN}$ |
| Program Verify | | $V_{IL}$ | $V_{IL}$ | X | X | $V_{PP}$ | $D_{OUT}$ |
| Program Inhibit | | $V_{IH}$ | X | X | X | $V_{PP}$ | HIGH Z |
| Auto Select (Note 3) | Manufacturer Code | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_H$ | X | 01h |
| | Device Code | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_H$ | X | 9Bh |

***Note:***

1. *$V_H$ = 12.0 V ± 0.5 V.*
2. *X = Either $V_{IH}$ or $V_{IL}$*
3. *A1 – A8 = A10 – A18 = $V_{IL}$*
4. *See DC Programming Characteristics in the EPROM Products Data Book for $V_{PP}$ voltage during programming*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature

OTP Products . . . . . –65°C to +125°C

All Other Products. . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . .–55°C to + 125°C

Voltage with Respect to $V_{SS}$

All pins except A9, $V_{PP}$, $V_{CC}$ (Note 1) . . . . . –0.6 V to $V_{CC}$ +0.5 V

A9 and $V_{PP}$ (Note 2) . . . . . .–0.6 V to +13.5 V

$V_{CC}$ . . . . . .–0.6 V to +7.0 V

1. *During voltage transitions, inputs may overshoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins may overshoot to $V_{CC}$ + 2.0 V for periods up to 20ns.*
2. *During voltage transitions, A9 and $V_{PP}$ may overshoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. A9 and $V_{PP}$ must not exceed +13.5 V at any time.*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) . . . . . .0°C to +70°C

**Industrial (I) Devices**

Ambient Temperature ($T_A$) . . . . . .–40°C to +85°C

**Extended (E) Devices**

Ambient Temperature ($T_A$) . . . . . .–55°C to +125°C

**Supply Read Voltages**

$V_{CC}$ for ± 5% devices . . . . . +4.75 V to +5.25 V
$V_{CC}$ for ± 10% devices . . . . . +4.50 V to +5.50 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –400 µA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.1 mA | | | 0.45 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input LOW Voltage | | | –0.5 | +0.8 | V |
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0 V to $V_{CC}$ | C/I Devices | | 1.0 | µA |
| | | | E Devices | | 5.0 | |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0 V to $V_{CC}$ | | | 5.0 | µA |
| $I_{CC1}$ | $V_{CC}$ Active Current (Note 3) | CE# = $V_{IL}$, f = 10 MHz, $I_{OUT}$ = 0 MA | C/I Devices | | 40 | mA |
| | | | E Devices | | 60 | |
| $I_{CC2}$ | $V_{CC}$ TTL Standby Current | CE# = $V_{IH}$ | | | 1.0 | mA |
| $I_{CC3}$ | $V_{CC}$ CMOS Standby Current | CE# = $V_{CC}$ ± 0.3 V | | | 100 | µA |
| $I_{PP1}$ | $V_{PP}$ Current During Read | CE# = OE# = $V_{IL}$, $V_{PP}$ = $V_{CC}$ | | | 100 | µA |

***Caution**: The device must not be removed from (or inserted into) a socket when $V_{CC}$ or $V_{PP}$ is applied.*

***Notes:***

1. *$V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$*
2. *$I_{CC1}$ is tested with OE# = $V_{IH}$ to simulate open outputs.*
3. *Minimum DC Input Voltage is –0.5. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is Vcc +0.5 V, which may overshoot to $V_{CC}$ +2.0 V for periods less than 20 ns.*

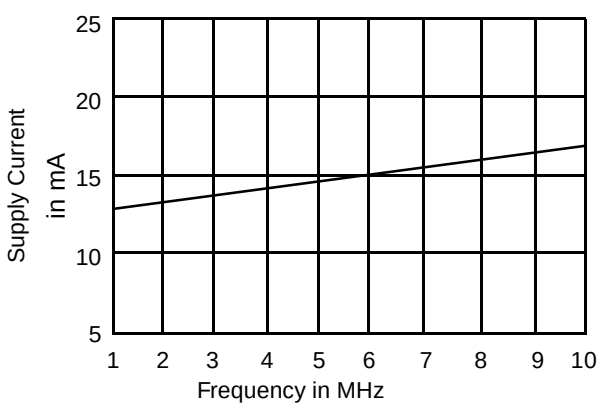



**Figure 1. Typical Supply Current vs. Frequency $V_{CC}$ = 5.5 V, T = 25°C**

14971E-1

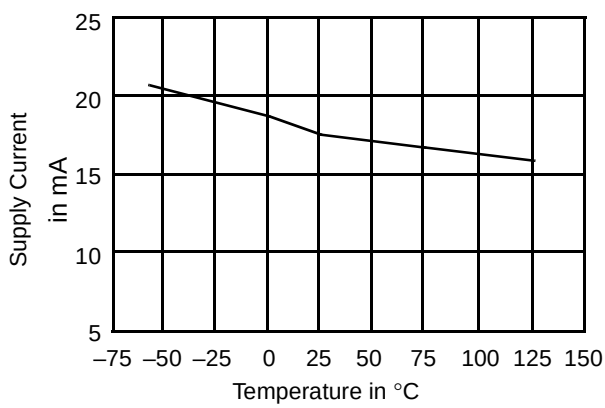
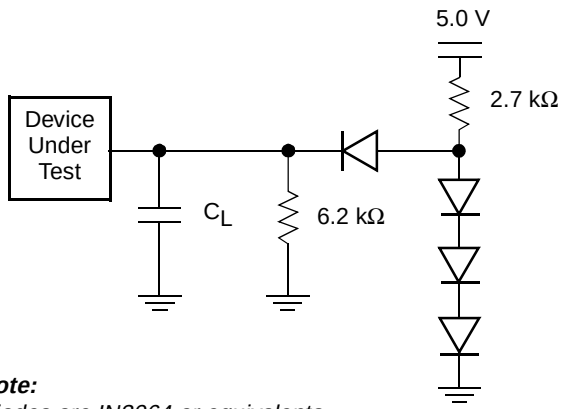



**Figure 2. Typical Supply Current vs. Temperature $V_{CC}$ = 5.5 V, f = 10 MHz**

14971E-1

## TEST CONDITIONS




***Note:***
*Diodes are IN3064 or equivalents.*

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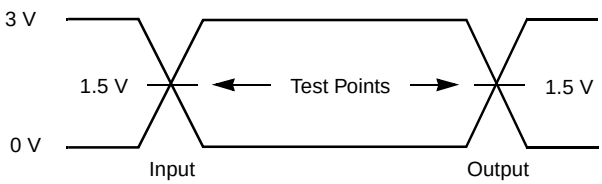
**Figure 1. Test Setup**

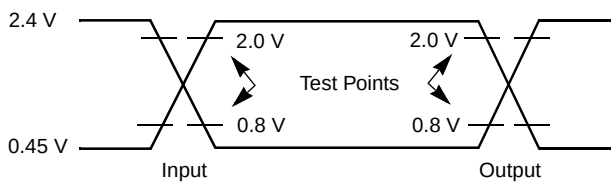
**Table 1. Test Specifications**

| Test Condition | All | Unit |
|---|---|---|
| Output Load | 1 TTL gate | |
| Output Load Capacitance, $C_L$ (including jig capacitance) | 100 | pF |
| Input Rise and Fall Times | ≤ 20 | ns |
| Input Pulse Levels | 0.45–2.4 | V |
| Input timing measurement reference levels | 0.8, 2.0 | V |
| Output timing measurement reference levels | 0.8, 2.0 | V |

## SWITCHING TEST WAVEFORM




***Note:*** *For $C_L$ = 30 pF.*




***Note:*** *For $C_L$ = 100 pF.*

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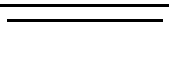
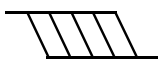
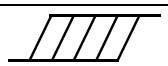
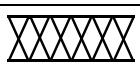
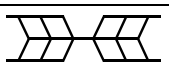
## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Steady | |
|  | Changing from H to L | |
|  | Changing from L to H | |
|  | Don't Care, Any Change Permitted | Changing, State Unknown |
|  | Does Not Apply | Center Line is High Impedance State (High Z) |

KS000010-PAL

## AC CHARACTERISTICS

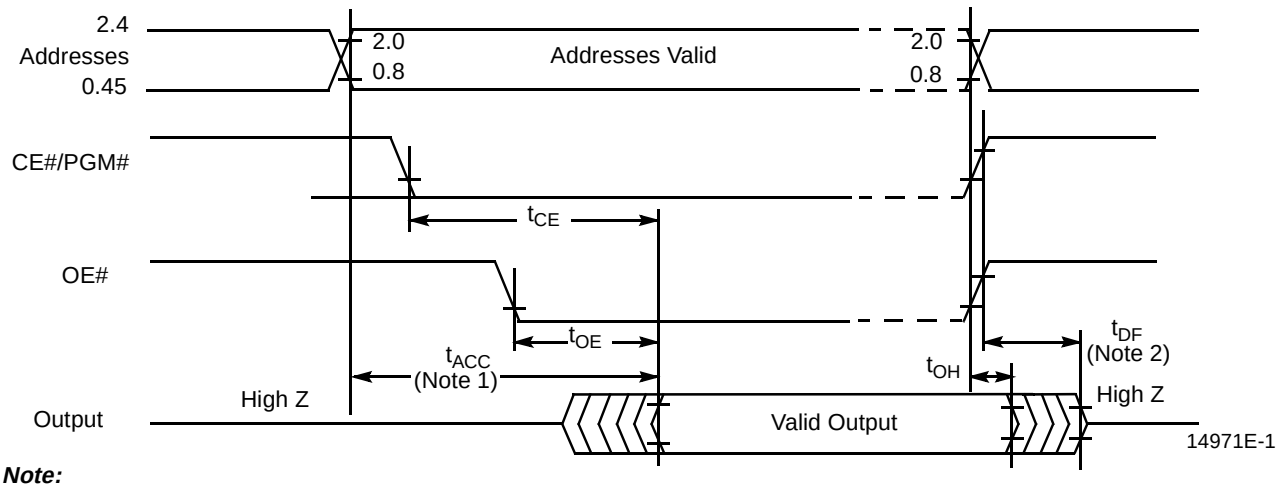
| Parameter Symbols | | Description | Test Setup | | Am27C040 | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | -90 | -120 | -150 | -200 | |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | CE# = OE# = $V_{IL}$ | Max | 90 | 120 | 150 | 200 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | OE# = $V_{IL}$ | Max | 90 | 120 | 150 | 200 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | CE# = $V_{IL}$ | Max | 40 | 50 | 65 | 75 | ns |
| $t_{EHQZ}$ $t_{GHQZ}$ | $t_{DF}$ (Note 2) | Chip Enable High or Output Enable High, Whichever Occurs First, to Output High Z | | Max | 30 | 30 | 30 | 40 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First | | Min | 0 | 0 | 0 | 0 | ns |

***Caution**: Do not remove the device from (or inserted into) a socket when $V_{CC}$ or $V_{PP}$ is applied.*

***Notes:***

1. *$V_{CC}$ must be applied simultaneously or before $V_{PP}$, and removed simultaneously or after $V_{PP}$*
2. *This parameter is sampled and not 100% tested.*
3. *Switching characteristics are over operating range, unless otherwise specified.*
4. *See Figure 1 and Table 1 for test specifications.*

## SWITCHING WAVEFORMS




***Note:***

1. *OE# may be delayed up to $t_{ACC}$ - $t_{OE}$ after the falling edge of the addresses without impact on $t_{ACC}$.*
2. *$t_{DF}$ is specified from OE# or CE#, whichever occurs first.*

## PACKAGE CAPACITANCE

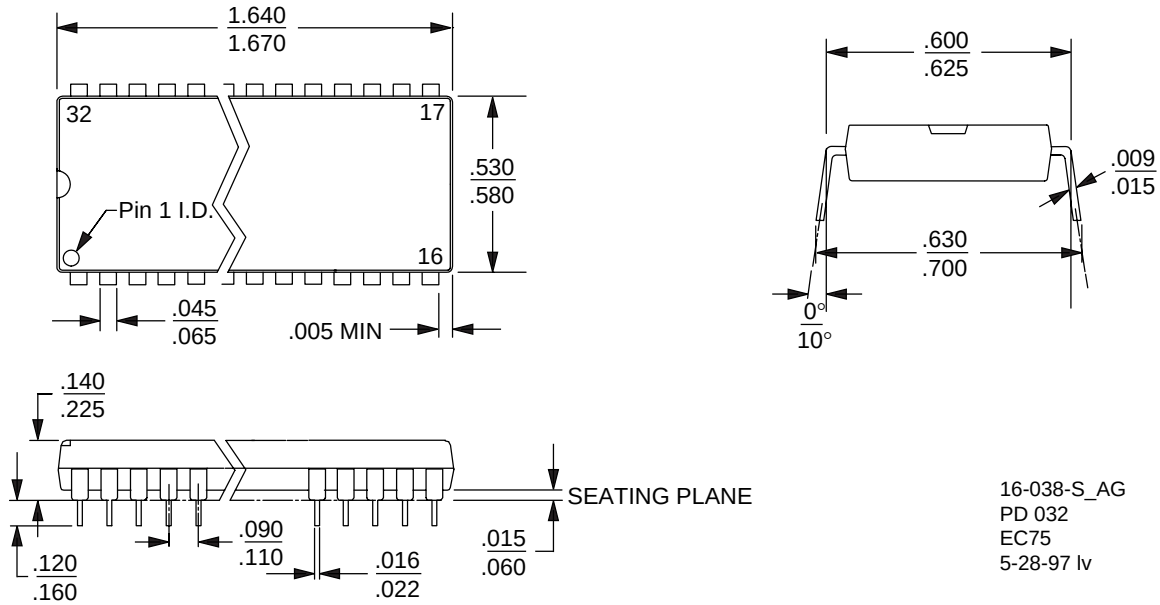
| Parameter Symbol | Parameter Description | Test Conditions | CDV032 | | PD 032 | | PL 032 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Typ | Max | Typ | Max | Typ | Max | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 V | 10 | 12 | 10 | 12 | 8 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V | 12 | 15 | 12 | 15 | 9 | 12 | pF |

***Notes:***

1. *This parameter is only sampled and not 100% tested.*
2. *$T_A$ = +25°C, f = 1 MHz.*

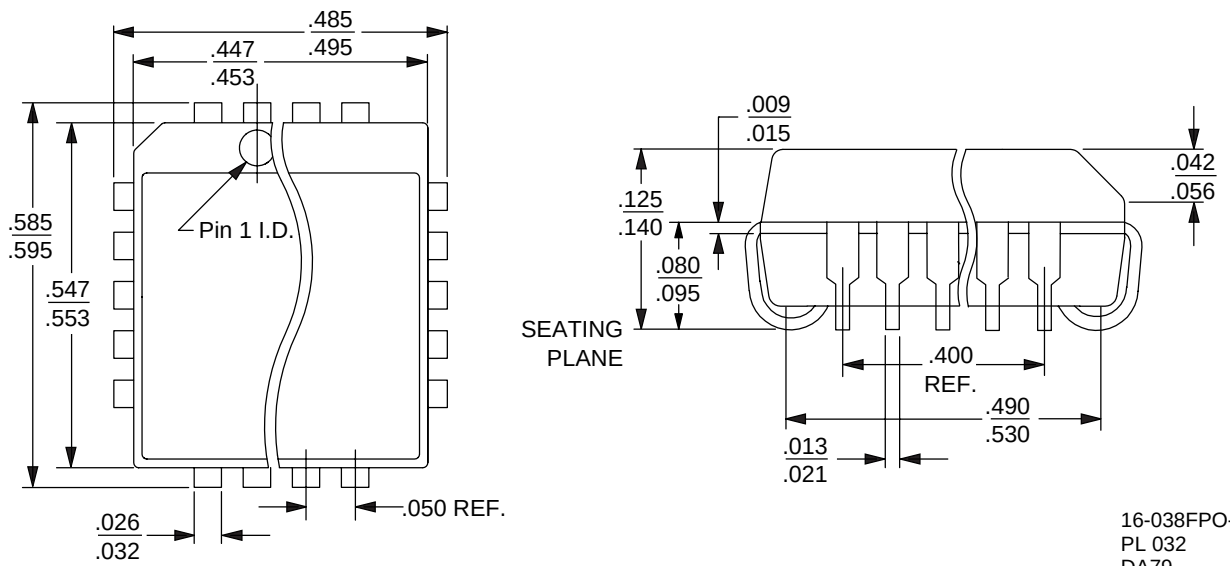
## PHYSICAL DIMENSIONS

### PD 032—32-Pin Plastic Dual In-Line Package (measured in inches)




16-038-S_AG
PD 032
EC75
5-28-97 lv

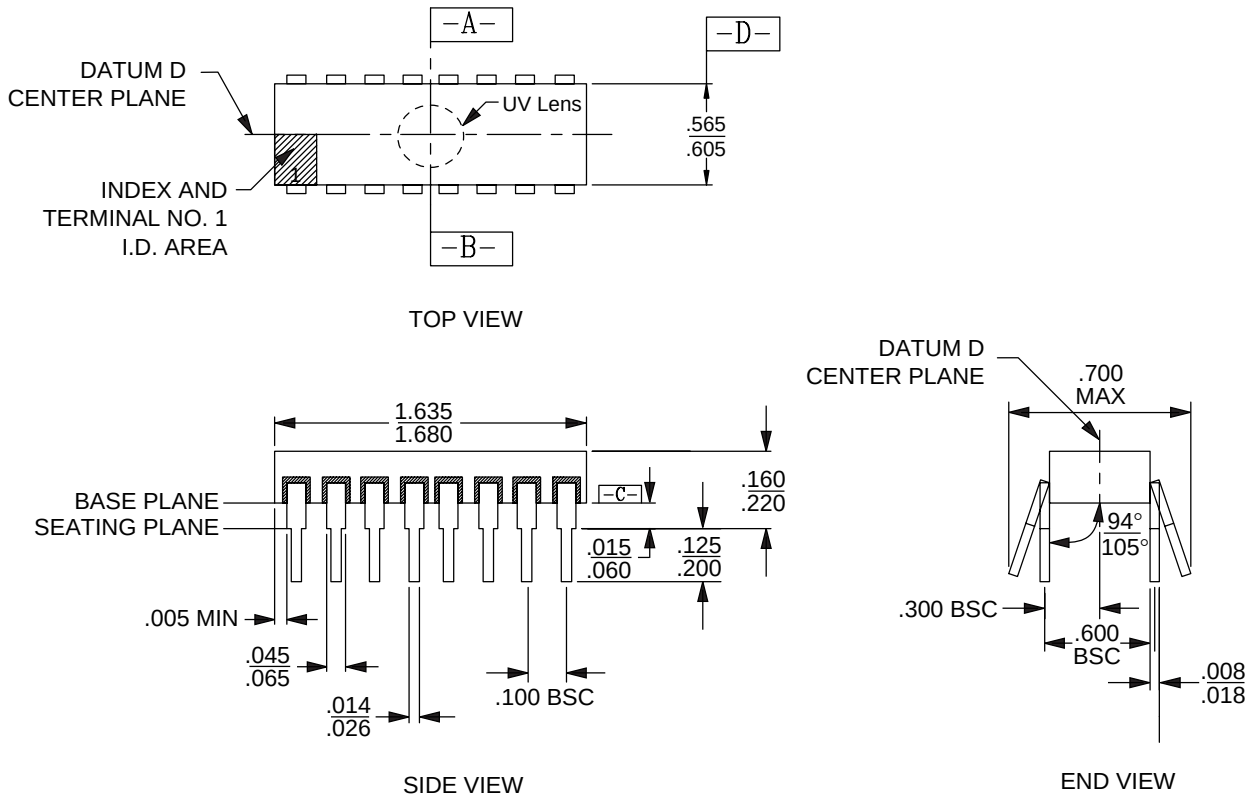
### PL 032—32-Pin Plastic Leaded Chip Carrier (measured in inches)




16-038FPO-5
PL 032
DA79
6-28-94 ae

## PHYSICAL DIMENSIONS*

## CDV032—32-Pin Ceramic DIP, UV Lens (measured in inches)




16-000038H-3
CDV032
DF11
3-30-95 ae

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

## REVISION SUMMARY

### Revision E/1 (November 1996)

**Product Selector Guide:**

Added -90 (90 ns, ±10% $V_{CC}$) and deleted -100 speed options.

**Ordering Information, UV EPROM Products:**

The -90 part number is now listed in the example.

*Valid Combinations:* Added -90 and deleted -100 speed options in valid combinations.

**Ordering Information, OTP EPROM Products:**

The -90 part number is now listed in the example.

*Valid Combinations:* Added -90 and deleted -100 speed options in valid combinations.

**Programming the Am27C040:**

The fourth paragraph should read, “Please refer to Section 5 for programming…”.

**Operating Ranges:**

Changed Supply Read Voltages listings to match those in the Product Selector Guide.

**AC Characteristics:**

Added -90 and deleted -100 speed options in table, re-arranged notes, moved text from table title to Note 4, renamed table.

### Revision F (October 1997)

Deleted -255 speed option.

Changed all active low signal designations from over-bars or trailing “#”s.

## Revision G (May 1998)

### Global

Made formatting and layout consistent with other data sheets. Used updated common tables and diagrams.

### Distinctive Characteristics:

*Low Power Consumption:* Changed “100 µA maximum” to “<10 µA typical”.

TSOP package deleted.

### General Description:

In the third paragraph, changed “100 µW in standby mode” to 50 µW in standby mode”.

### Connection Diagrams:

Deleted TSOP Pinout figure.

### Pin Designations:

Changed “Chip Enable Input” to “Chip Enable/Program Enable Input”.

### Ordering Information:

*UV EPROM Products:* Changed -75 speed option to -90.

*OTP EPROM Products:* Changed -75 speed option to -90.

*Temperature Range:* Added “E = Extended (–55°C to 125°C)”.

*Package Type:* Deleted “E = 32-pin Thin Small Outline Package (TSOP) Standard Pinout (TS 032)”.

*Valid Combinations:* Deleted EC and EI options.

### Functional Description:

Replaced device specific text with generic text.

### Test Conditions:

New section with Test Setup Figure and Test Specifications Table.

### Switching Test Waveform:

Modified figure.

### Operating Ranges:

*Supply Read Voltages:* Replaced with generic data.

### DC Characteristics:

Modified Figures 1 and 2.

### Switching Waveform:

Corrected “DF” to “$t_{DF}$” in Note 2.

### Package Capacitance:

Deleted TSOP data.

### Physical Dimensions:

New section, added figures for the 32-Pin Ceramic DIP, 32-Pin Plastic DIP, and 32-Pin Plastic Leaded Chip Carrier.

## Revision H (August 25, 1999)

### Functional Description

*Device Erasure:* Changed the dosage from 15W to 30W. Changed the exposure time from 15–20 minutes to 30–35 minutes.

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